6,028,983 (hereinafter "Jaber"). Applicants respectfully traverse this §103(a) rejection, for the reasons specified below.

A proper *prima facie* case of obviousness requires that the cited references when combined must "teach or suggest all the claim limitations," and that there be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references or to modify the reference teachings. See Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §706.02(j).

Applicants submit that the Examiner has failed to establish a proper *prima facie* case of obviousness in the present §103(a) rejection, in that the Spix and Jaber references, even if assumed to be combinable, fail to teach or suggest all the claim limitations, and in that no cogent motivation has been identified for combining the references or modifying the reference teachings to reach the claimed invention. Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner.

Each of independent claims 1, 13, 19 and 20 involves testing a digital system comprising a plurality of processors, and includes limitations relating to defining at least a subset of the processors as forming a group of processors to be subject to common control and delaying issuance of one or more commands for the group until a group scan command is received for each of the processors in the group.

The present invention as set forth in these claims provides a number of significant advantages over conventional approaches. For example, the claimed arrangements allow the multiple processors to perform synchronous or pseudo-synchronous operations without requiring excessive coupling between individual processor debug systems as in the conventional approaches. In addition, the processor grouping can be altered dynamically to allow for multiple groups of processors on the same scan chain and the alterations of these groups during a single debugging session. This control mechanism of the present invention is thus reusable for different numbers and arrangements of processors.

Applicants submit that the proposed combination of Spix and Jaber fails to teach or suggest at least the above-noted limitations of each of independent claims 1, 13, 19 and 20, and furthermore fails to provide the associated advantages of the claimed invention.

The Examiner in formulating the § 103(a) rejection acknowledges that Spix "does not disclose the use of a group scan command," and thus fails to teach or suggest an arrangement in which the issuance of one or more commands for a group of processors subject to common control is inhibited or otherwise delayed until a group scan command is received for each of the processors in the group. See the Office Action at page 3, line 3. However, the Examiner argues that such an arrangement would be obvious in view of Spix and the teachings in Jaber at column 3, lines 54-56, and column 4, lines 6-7 and 16-22. Applicants respectfully disagree. The relied-upon teachings from Jaber provide as follows, with emphasis supplied:

Another object is an improved test apparatus and method of operation which limits voltage swings in scan testing of high-performance microprocessor chips.

. . .

Another object is an improved JTAG port in scan testing of a microprocessor chip.

These and other objects, features and advantages are achieved in a test apparatus for design verification of at least one microprocessor chip having a compatible Joint Task Action Group (JTAG) terminal. A plurality of computer functional units are contained in the chip for testing of design verification through the compatible JTAG terminal. A test input terminal included in the JTAG terminal receives a scan string, the string being coupled to each computer functional unit through a first multiplexer. The scan input string is divided into a series of dedicated scan strings, each dedicated scan string being supplied to a selected functional unit through the first multiplexer. Each functional unit includes start and stop scan clocks for entering the dedicated scan string into the functional unit for test purposes.

Applicants submit that these teachings not only fail to meet the claim limitation that calls for delaying the issuance of one or more commands for a group of processors subject to common control

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until a group scan command is received for each of the processors in the group, but in fact directly teach away from it. More specifically, by teaching that each functional unit includes its own start and stop clocks for processing a corresponding dedicated scan string portion of an input scan string, Jaber teaches away from the particular claimed arrangement involving delaying the issuance of one or more commands for a group of processors. This is further apparent from the passage at column 4, lines 26-35 of Jaber, which provides as follows:

> The compatible JTAG terminal includes further means for controlling the scan clocks to select a targeted functional unit for testing purposes while the scan strings for non-targeted functional units remain in an inactive state. By limiting the functional units under test, the voltage swing in the chip is reduced for test purposes; scan time for testing is decreased; memory space allocation for storing test results is reduced and design verification is not delayed by the loss of access to functional units due to a break in the scan signal.

The cited portions of Jaber appear to relate to independent control of the functional units. The relied-upon teachings thus fail to disclose the claimed arrangement in which the issuance of one or more commands is delayed, for a group of processors subject to common control, until a group scan command is received for each of the processors in the group.

Applicants respectfully submit that neither Spix nor Jaber provides any teaching or suggestion whatsover regarding the claimed group scan command. As Applicants indicated in their previous response, one possible example of such a group scan command in an illustrative embodiment of the present invention is described as follows at page 6, lines 1-9 of the specification:

> A group scan command in the illustrative embodiment refers generally to a final JTAG scan command that occurs before a desired synchronous or pseudo-synchronous behavior. The group scan command generated by one of the TAP managers in a group is delayed by the chain manager 106 until the TAP managers for all other group members issue a group scan command. The individual commands of the groups are then merged, and

synchronously and simultaneously scanned into the scan chain 110 by the chain manager 106.

The chain manager 106 thus delays the issuance of the group scan commands for the members of the group until all members of the group arrive at an equivalent state in their control sequences.

As noted above, the Examiner acknowledges that Spix "does not disclose the use of a group scan command" as claimed. Moreover, based on a search conducted by the undersigned in an electronic version of the Jaber reference taken from the database at the USPTO web site, the phrases "group scan" or "group scan command" apparently do not appear anywhere in the text of the Jaber reference. It is difficult to imagine how one could reasonably argue that Spix and Jaber collectively meet the group scan command limitation in question when neither reference makes any mention whatsoever regarding a group scan or a group scan command.

Each of claims 1, 13, 19 and 20 thus includes one or more limitations which are not taught or suggested by the proposed combination of Spix and Jaber. The combined teachings of these references therefore fail to "teach or suggest all the claim limitations" as would be required by a proper §103(a) rejection.

Also, as indicated previously, the Examiner has failed to identify a cogent motivation for combining the references or for modifying the reference teachings to reach the claimed invention.

Applicants initially submit that Spix and Jaber are in fact non-analogous art relative to one another. Spix is in the field of "maintenance and control of computer systems" and more specifically relates to "an integrated system for controlling and maintaining a high-speed supercomputer and its peripheral devices using a number of maintenance control units" (Spix, column 1, lines 24-30). The Jaber reference, by contrast, is in the integrated circuit scan testing art (Jaber, column 1, lines 7-10). One looking for teachings regarding scan testing of circuits or systems would not be motivated, absent some explicit suggestion, to look toward the supercomputer maintenance and control art. This disparity in the technical fields of Spix and Jaber is indicative of a lack of motivation to combine the references.

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As was described above, neither Spix nor Jaber teaches or suggests the limitation of claims 1, 13, 19 and 20 that calls for delaying the issuance of one or more commands for a group of processors subject to common control <u>until a group scan command is received for each of the processors in the group</u>. However, the Examiner argues that it would be obvious to combine or modify the teachings of these references to meet the limitation in question. The statement of obviousness provided by the Examiner at page 3, lines 5-8 of the Office Action is as follows:

> It would have been obvious to one of ordinary skill in the art at the time of the invention to include means to combine the Jaber reference with the Spix reference. Spix discloses that it would be useful for setting and sensing capability in a highly parallel processing system.

<u>Applicants submit that this is a conclusory statement of obviousness, and insufficient to support the proposed combination or modification of the reference teachings</u>.

The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344. There has been no showing in the present § 103(a) rejection of objective evidence of record that would motivate one skilled in the art to combine Spix and Jaber or to modify the proposed combination of Spix and Jaber to produce the particular limitations in question. Instead, the Examiner points to column 3, lines 22-27 of Spix, which provides as follows:

> It is clear that there is a need for a control and maintenance architecture specifically designed for the needs of a highly parallel multiprocessor system. Specifically, there is a need for a maintenance subsystem allowing setting and sensing capability for all internal

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machine registers, the ability to set and sense machine states by management of massive amounts of information, independent control of processor power up sequences, processor clocks, processor machine states, and peripheral devices.

Although this passage may be a motivation for the specific invention described in Spix, it fails to provide the requisite motivation for the proposed combination of Spix with an integrated circuit scan testing reference such as Jaber.

The above-quoted statement of obviousness given by the Examiner in the Office Action is thus believed to be precisely the type of subjective, conclusory statement that the Federal Circuit has indicated provides insufficient support for an obviousness rejection. It appears, in view of the above-quoted conclusory statement of obviousness provided by the Examiner, that the Examiner in combining Spix and Jaber has simply undertaken a hindsight-based piecemeal reconstruction of the claimed invention based on the disclosure provided by Applicants. Such an approach is improper.

Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner. For example, the Jaber reference, in accordance with the previously-described teachings from column 4, lines 6-35 thereof, teaches to limit the functional units under test by controlling the scan clocks <u>to select a targeted functional unit for testing purposes while the scan strings for non-targeted functional units remain in an inactive state</u>. It is believed that this is a direct teaching away from the claimed invention, which calls for delaying the issuance of one or more commands for a group of processors subject to common control <u>until a group scan command is received for each of the processors in the group</u>. Such a teaching away constitutes evidence of non-obviousness.

Applicants therefore respectfully submit that independent claims 1, 13, 19 and 20 are allowable over Spix, Jaber and the other art of record. The § 103(a) rejection of independent claims 1, 13, 19 and 20 over Spix and Jaber is therefore believed to be improper, and should be withdrawn.

Independent claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Spix and Jaber in view of U.S. Patent No. 6,263,373 (hereinafter "Cromer"). Claim 15 includes

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limitations similar to those of claims 1, 13, 19 and 20, and is therefore believed allowable for at least the reasons identified above. The Cromer reference fails to supplement the fundamental deficiencies of the proposed combination of Spix and Jaber with regard to these limitations. The Spix, Jaber and Cromer references, even if assumed to be combinable, fail to teach or suggest all of the limitations of claim 15. The §103(a) rejection of independent claim 15 over Spix, Jaber and Cromer is therefore believed to be improper and should be withdrawn.

Dependent claims 2-12, 14 and 16-18 are believed allowable for at least the reasons identified above with regard to their respective independent claims. The rejections of these claims should therefore also be withdrawn. Moreover, one or more of these dependent claims are believed to recite additional separately-patentable subject matter over the cited references.
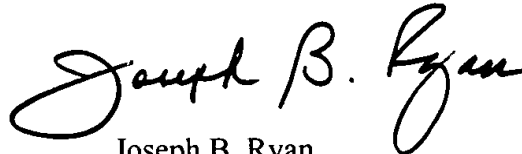
For example, dependent claim 2 calls for defining a group of processors in a chain manager in response to a group request received from a debugger. The Examiner argues that this limitation is obvious in view of Spix, Jaber and U.S. Patent No. 6,108,699 (hereinafter "Moiin"). However, the collective teachings of the cited references fail to meet the particular language of the limitation in question.

As another example, dependent claim 3 calls for a chain manager that establishes a group identifier for the group, stores the group identifier and a size of the group, and returns the group identifier to the debugger. Again, the Examiner argues that this limitation is obvious in view of Spix, Jaber and Moiin, when the collective teachings of these references fail to meet the particular language of the limitation in question.

In view of the above, Applicants believe that claims 1-20 are in condition for allowance, and respectfully request withdrawal of the §103(a) rejections.

As indicated previously, a Notice of Appeal is submitted concurrently herewith. Since the claims have been twice rejected, Applicants have a right to appeal in accordance with 37 C.F.R. §1.191(a).

Respectfully submitted,

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Enclosure: Notice of Appeal